計算機組織 HW3

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4.9.1

100011 00110 00001 0000000000101000

4.9.2

Read register 1 00110 yes

Read register 2 00001 yes

4.9.3

Write register 00001 yes

4.9.4

RegDst = 0

MemRead = 1

4.11.1

Sign-extend 00000000000000000000000000010000

Jump’s shift left 2 00010000110000000001000000

4.11.2

ALUop 00 Instruction 010000

4.11.3

PC + 4

4.11.4

WrReg Mux ALU Mux Mem/ALU Mux Branch Mux Jump Mux

0 16 1 PC+4 PC+4

4.11.5

ALU add(PC+4) add(branch)

2,16 pc,4 PC+4,16\*4

4.11.6

Readreg1 readreg2 wrreg wrdata regwrite

2 3 3 0 1

4.16.1

4.16.2

$1,$6

實際讀取$1,$6

4.16.3

EX 40+$6

MEM 從内存讀取value

4.18.1

EX ALUSrc = 0

ALUop = 10

RegDst = 1

MEM Branch = 0

MemWrite = 0

MemRead = 0

WB MemtoReg = 0

RegWrite = 1

4.18.2

1 clock cycle

4.18.3

PCSrc = 0

4.18.4

Signal 1 ID生成 EX使用

Signal 2 ID生成WB使用

4.18.5

R-type

4.18.6

不是time-travel paradox

4.20.1

Instruction Seq RAW WAR WAW

I1: lw $1, 40($2) ($1) I1 to I3 ($2)I1 to I2 ($1)I1 to I3

I2: add $2, $3, $3 ($2)I2 to I3, I4 ($1)I3 to I4 ($1)I3 to I4

I3: add $1, $1, $2

I4: sw $1, 20($2)

4.20.2

Instruction Seq With Forwarding Without Forwarding

i1: lw $1, 40($2) ($1) I1 to I3

I2: add $2, $3, $3 ($2)I2 to I3, I4

I3: add $1, $1, $2

I4: sw $1, 20($2)

4.20.3

Instruction Seq With Forwarding Without Forwarding

I1: lw $1, 40($2) ($1) I1 to I3 ($1) I1 to I3

I2: add $2, $3, $3 ($2)I2 to I3, I4

I3: add $1, $1, $2

I4: sw $1, 20($2)

4.23.1

3\*(1-0.4)\*0.15=0.27

4.23.2

3\*(1-0.6)\*0.15=0.18

4.23.3

3\*(1-0.8)\*0.15=0.09

4.24.1

Always-taken 75%

Always-not-taken 25%

4.24.2

Outcomes Predictor Value at Time of Prediction Correct or Incorrect Accuracy

T, T, NT, T 0, 1, 2, 0 I, I, I, I 0%

4.24.3